IN THE SPECIFICATION

Please replace the paragraph bridging pages 6-7 with the following:

Referring now more particularly to Fig. 1, there is shown a semiconductor substrate 10. Deep trench capacitor 24 has been formed partially underlying shallow trench isolation 28. Gate electrodes and interconnection lines 30 and bit lines 36 have been formed overlying the semiconductor substrate. Buried strap 40 forms diffusion junction 42. L is the buried strap height defined by (recess 2 - recess 3) in the conventional scheme. W is the buried strap width defined by the overlap between the deep trench and the active area. The junction depth of the buried strap diffusion junction 42 is a function of the buried strap height, temperature, and time during the post recess anneal step. Buried strap resistance is a function of the doping concentration of the second polysilicon layer, the buried strap junction depth, and buried strap width. It is desired to have a minimal buried strap resistance which defines drain sheet resistance.

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Please replace the first full paragraph on page 10 through the top of page 12 with the following:

The preferred selective HSG polysilicon process will now be described. Preferably, the optional surface amorphization step by plasma doping has been performed to provide surface mobility of the silicon atoms in 54 to promote HSG formation. Now, selective HSG 62 is formed as is conventional in the art for stacked capacitor applications.

The polysilicon 62 (or other conductive layer) can be doped in-situ during or immediately after the deposition step. Alternatively, the polysilicon layer 62 can be doped after deposition using plasma doping, plasma ion immersion implantation (PIII), or gas phase doping (GPD) for fine dose control. Fig. 7 illustrates the alternative post-deposition doping step 65. Doping (in-situ or post-deposition) uses arsenic or phosphorus ions for a doping concentration of between about 1E18 to 1E21 ions/cm^3.

The polysilicon layer 62 formed by HSG has a thickness of between about 20 and 100 nm and a grain size of between about 10 and 50 nm. This HSG layer will form the buried strap of the present invention. The selective HSG

polysilicon deposition method deposits the buried strap polysilicon to a controlled thickness. This process avoids planarization of the buried strap layer by CMP which adds process complexity.

Optionally, a capping layer 64 may be formed over the buried strap 62, as shown in Fig. 8. The optional capping layer 64 may be used to suppress dopant loss or to minimize the surface stress which might cause dislocation into the crystalline silicon substrate. A trench top oxide or other capping layer such as silicon nitride 64 may be deposited using a selective oxidation method or by an unbiased silicon nitride liner method, whichever is appropriate for a chosen integration method, to a thickness of between about 10 and 20 nm. This additional layer may serve as a sacrificial capping layer against any contamination during or after the integration steps such as annealing or implantation steps.

Please replace the first paragraph on page 13 with the following:

The silicon nitride layer 14 is stripped using a wet etching process. Now, a gate oxide layer 80 is grown on the substrate surface in the active area, as shown in Fig. 14. Gate electrodes 84 are formed as is conventional in the art. Buried strap diffusion junction 86 is formed by outdiffusion from the buried strap 62 during thermal processes. The diffusion junction 86 provides a connection between the deep trench capacitor 54 and the transistor 84.